1 The Intermediate STAR Tracker

The Intermediate Silicon Tracker (IST) consists of a barrel of approximately 0.4m^2 of silicon pad sensors at a radius of 14 cm. The sensors are supported by 24 carbon fiber ladders, which are tiled for maximum hermiticity. Figure 1 shows a SolidWorks model of the IST. Table 1 gives the most relevant specifications.

Radius	14 cm
Length	50 cm
Number of ladders	24
Number of hybrids	72
Number of sensors	144
Number of readout chips	864
Number of channels	110592
R-ϕ resolution	172 μm
Z resolution	1811 μm

Table 1: Specifications for the IST.

Together with the Silicon Strip Detector(SSD) the IST provides the intermediate space points that ties the tracking in the Time Projector Chamber (TPC) and the tracking in the 2 PIXEL layers together. The best figure-of-merit for the total Heavy Flavor Tracker tracking capabilities is the final D^0 reconstruction efficiency. Determining this efficiency involves extensive GEANT simulations and analysis. However, for the IST and the SSD, it is sufficient to optimize these layers for a high HFT+TPC single track reconstruction efficiency. How IST and SSD work together with PIXEL and TPC to reconstruct single tracks is a major ingredient for the final D^0 reconstruction efficiency. However, the actual D^0 reconstruction is the sole task of the 2 PIXEL layers. To optimize the HFT single track efficiency a fast simulation code was used to determine the optimum radius of the IST barrel and the internal geometry of the silicon pad sensors. Section 1.1 discussed these choices in detail.

The IST has to be fast enough to work together with other, sometimes already existing, STAR detectors. It should also be able to function propery still after being irradiated during its projected lifetime. Section 1.2 describes, amongst others, the constraints on the IST by the experimental requirements and the subsequent hardware choices.

Section 1.3 gives an overview of the chosen hardware components. This section focusses on the components which are locates on the IST barrel. The readout and slow controls are described in section 1.4.

Since the IST is part of an accurate tracking device its internal and external spatial alignment are discussed separately in section 1.5.

1.1 IST Optimized Geometry

The Intermediate Silicon Tracker is located between the outer layer of the PXL detector and the SSD. Taking mechanical constraints into account a possible radius range is from 12 to 20 cm. This radius has to be optimized for reconstruction efficiency while keeping the SSD and IST redundancy in mind. The IST barrel will cover the full acceptance of the STAR TPC, i.e. 2π coverage for $-1 < \eta < +1$.

At the highest RHIC energy of 200 GeV for Au+Au collisions the charged particle density at a radius of 12 cm can easily exceed one per cm^2. The silicon sensors need to be divided into pads such that the occupancy of the individual pads do not exceed a few percent. The occupancy is fully

determined by the number of active elements and can be reached by different sensor geometries. What has to be taken into account is the double-hit probability within the search area on the IST sensors resulting from the pointing resolution of the TPC and SSD. Figure 2 shows the occupancy of a sensor with 768 active elements and the fraction of hits that are accompanied by one or more hits in the search area. In the case of a silicon strip detector the search area is defined by the width of the search area and the length of the strips. At the proposed radius of 14 cm more than 10% of the tracks would result in ambiguous IST hits. For the proposed silicon pad sensors this drops to about 1%. The number of active elements is determined by the density, with which the readout chips can be packed on the hybrids.

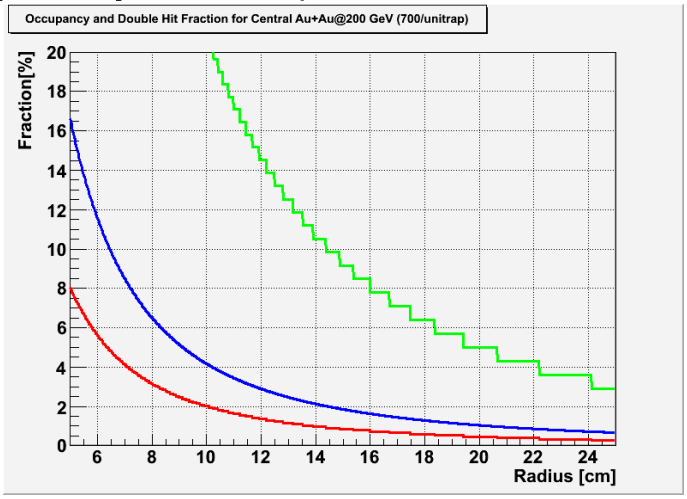

Figure 1: Occupancy [blue curve] and double-hit fraction for a silicon strip detector [green curve] and a silicon pad sensor [red curve].

Silicon pad sensors are well suited to the RHIC environment and proved their suitability in the PHOBOS experiment. Figure 3 shows a study of the single track finding efficiency of the HFT as a function of the pad layout of the IST sensors. The better resolution (the size of the pads on the y-axis) is in R-ϕ, the bending plane. From these studies it was determined that 768 channels arranged in strips of roughly 600 µm x 6000 µm provide an efficiency of about 83%. Going to more channels could give a slightly better efficiency but would lead to space problems when trying to mount more readout chips on the hybrids. The right plot shows the efficiency when hits from the SSD are not included in the tracking. In this case the single track finding efficiency decreases to 73%. This has to be compared to 50% if the IST would not be there and only the TPC would provide tracking to the PXL. Thus, the IST adds in an essential way to the efficiency and redundancy of the HFT.

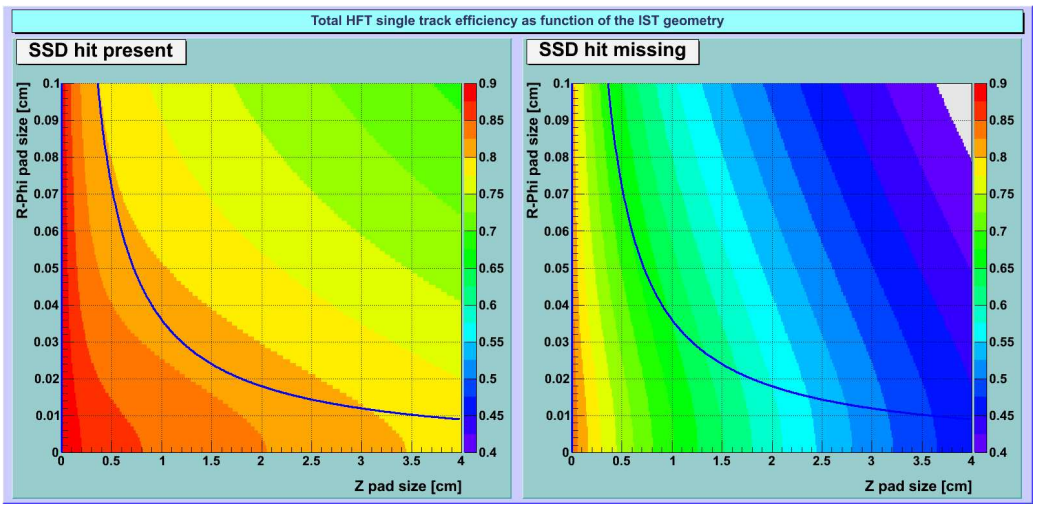

Figure 2: Single track finding efficiency for different R-ϕ and Z pad sizes of the IST. The solid line shows an iso-line for 768 readout channels. The left panel shows the efficiency when hits from the SSD are included. In the right panel the SSD hits are not included in the track. Particles tracked are kaons at 750 MeV/c.

The efficiency of the whole inner tracking system is determined by an intricate interplay of the detector layer radii, resolutions and thicknesses. Since these characteristics are mostly fixed for PXL and SSD, varying the radius of the IST barrel for a certain internal sensor geometry makes it possible to optimize the radius with respect to the single track efficiency quickly. Figure 4 shows a calculation of the single-track efficiency as a function of the IST barrel radius. Although the dependence is rather weak it is clear that 14 cm will give the best efficiency. This can be understood from the fact that IST is located roughly halfway between the outer layer of the PXL and the SSD.

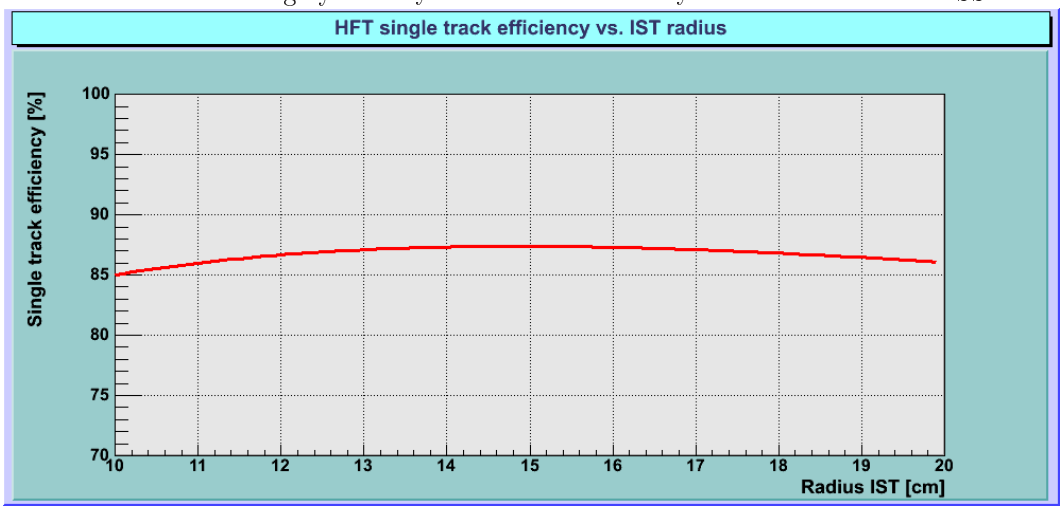

Figure 3: Single-track efficiency as a function of the IST barrel radius. The assumed internal sensor geometry was 600 μm in R-ϕ and 6000 μm in Z.

1.2 Experimental Requirements

The most relevant experimental constraints are data taking rate capabilities, radiation levels and the material budget. The data rate and radiation levels are constrained by the RHIC environment and have to be taken into account in the sensor and readout chip choice. The material budget is connected to the tracking capabilities of the inner tracking system, but has also a large impact

on the capabilities of more outward located detectors and their associated physics programs. The requirement to design a low mass IST with sufficient mechanical rigidity has led to the choice of state-of-the-art materials.

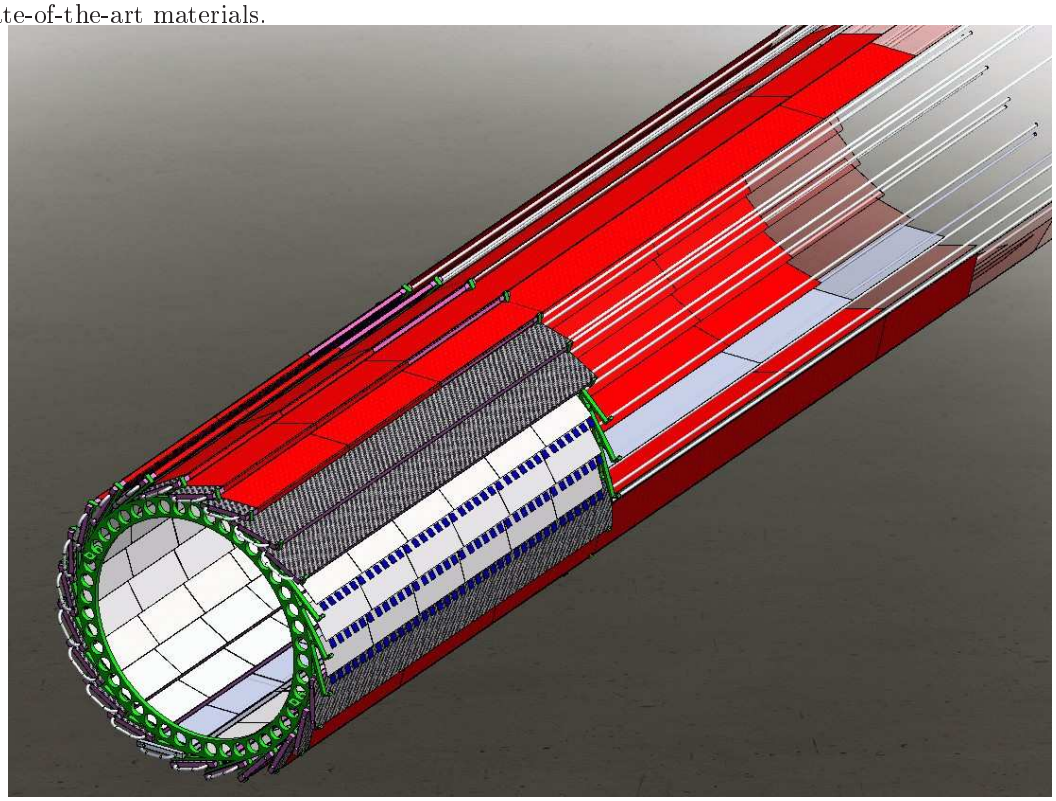

Figure 4: SolidWorks model of the IST.

The IST should be able to operate without significant event pile-up for 200 GeV Au+Au collisions. Therefore, the IST has to be able to resolve interactions from each beam bunch crossing which are occurring every 107 ns. The spin program at RHIC relies on individual beam bunch crossings to set and determine the relative spin orientations in the proton beams. Also here the IST has to be able to resolve individual beam bunches.

The intrinsic resolution of the IST is required to provide sufficient pointing accuracy for the PXL layers. This is more critical in R-ϕ compared to the Z direction. A resolution at the level of 200 μm in the R-ϕ plane will provide the needed pointing accuracy as discussed earlier.

Extrapolating the radiation doses received by the RHIC experiments during the past RHIC operations, it is expected that the total radiation dose for the IST barrel will not exceed 30 kRad per year. Both the silicon sensors and the readout chips on the hybrids are required to be fully operational after 10 years of operation.

The mass requirements for the IST are defined by the heavy ion physics requirements in the mid-rapidity region and by the W$-$boson spin physics program for more forward rapidities. To make the multiple Coulomb scattering comparable to the detector resolution the thickness of the IST layer has to be less than or equal to 1.5% of a radiation length.

Readout Chips

The APV25-S1 chip was chosen for reading out the IST sensors because it met the requirements and is readily available. This readout chip was developed for the CMS silicon tracker, which is using about 75,000 of these chips. The radiation hard production process of the APV25-S1 will enable to withstand at least 2 orders of magnitude more in radiation load compared to what is expected to be accumulated during the lifetime of the IST. The chip is fast enough to handle the RHIC interaction clock, even with multiple interactions during p+p running. Moreover, the chip is already used

successfully for reading out the COMPASS triple-GEM detectors and will also be used to read out the STAR Forward GEM Tracker (FGT).

Hybrids and Ladders

To meet the requirement of the IST to have on average a thickness of less than 1.5% X_0, special attention has to be paid to the choice of materials for the hybrids, cables and ladders. For the cables Kapton with copper conductors was chosen. Although aluminum conductors would make the cables even lighter, they also would make them more difficult to produce and much more fragile. The radiation length requirement makes it not desirable to use a ceramic substrate, like AlN, for the hybrid. A 500 μm thick AlN substrate would already contribute 0.6% X_0 while being extremely fragile. A 250 μm thick G10 substrate would only add 0.13% X_0, but still the Kapton cable would have to be connected to this hybrid. Manufacturing the hybrid and cable out of one piece of Kapton circumvents connection problems and was chosen as the most elegant solution. Since the 50 µm thick Kapton is not self-supporting a proper supporting material is required. Using 250 µm thick carbon fiber leads to a thickness of 0.11% X_0 while providing the required mechanical rigidity.

A honeycomb carbon fiber structure with carbon fiber skins was chosen for the IST ladders. These use the same construction techniques and facilities as used for the ATLAS silicon tracker upgrade and add about 0.4% X_0 to the IST layer, including liquid cooling. Copying the ATLAS design in the same facility greatly reduces the engineering effort and cost of the ladders. Also, since the IST ladders are only half the length (50 cm) of the ATLAS ladders, the design is conservative with respect to strength and gravitational sag.

Cooling

The expected heat dissipation for the IST is 11 W per ladder, 264 W for the whole system. Although an air cooling system probably will be able to cool the IST, it is felt that a liquid cooling system will be able to perform this function in a more consistent way. A liquid cooling system will add at most 0.2% X_0 to the system.

Readout System

The Forward GEM Tracker is also using APV25-S1 readout chips. This system will be operational 2 years before the IST. In order to reduce the electronic engineering effort and to unify as many STAR readout systems as possible, the IST will use as much as possible of the FGT readout system. An effort is being made to design the FGT readout system such that it can be used also for the IST with as few alterations as possible.

1.3 IST Components

1.3.1 The Silicon Pad Sensors

The manufacturing techniques for silicon sensors are well established and are mastered by several manufacturers. The preference is to produce single sided devices with p-implants on n-bulk silicon using poly-silicon resistors. Such sensors are relatively easy to produce with high yield and can also be handled without much difficulty in a standard semiconductor lab. In contrast, double-sided devices have a lower yield (thus more expensive) and need special equipment to handle them.

Figure 5 shows the internal layout of the IST silicon pad sensors. The active elements are arranged in such a way that the best resolution is in the bending direction, i.e. R-ϕ. Along the beam direction, the resolution will be ten times larger. The sensors will be roughly 7.7 cm x 4 cm with 768 channels. All channels are AC coupled and connected through a second metal layer to bonding pads on one long edge of the sensor. From the manufacturing point of view this design is reasonably standard. Preliminary discussions with Hamamatsu showed that they are able to produce such sensors within the proposed budget.

Hamamatsu is the preferred vendor because of their excellent track record with respect to the quality of their produced sensors. This will greatly reduce the amount of quality control that has to be performed for these sensors. It will be sufficient to fully measure the characteristics of one or two samples per produced batch of about 20 sensors. Moreover, Hamamatsu uses design rules,

which make their sensors radiation hard. Therefore, we foresee no performance degradation during the expected IST lifetime.

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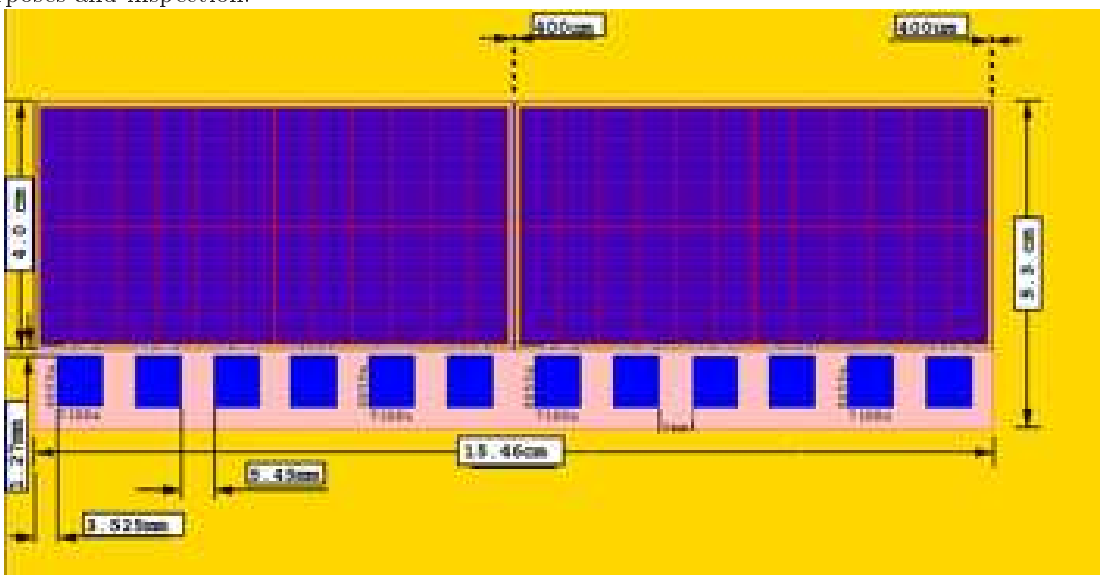
Figure 5: The silicon pad sensor internal layout.

1.3.2 The Readout Chips

About 100k channels will be read out in the IST. Readout chips with the necessary requirements for this system are already being used for similar purposes by other experiments. We chose the APV25-S1 readout chip.[1] Each channel of the APV25-S1 chip consists of a charge sensitive amplifier and shaper whose output signal is periodically sampled at up to 40 MHz (the LHC interaction rate). The samples are stored in a 4 μs deep analog pipeline. Following a trigger, the data in the pipeline can be processed by an analog circuit, mainly de-convoluting the amplifier response from the actual signal and associating the signal with a specific bunch crossing. The resulting analog data can then be multiplexed and sent to digitizer boards. Although the analog data lead to higher data volumes at the front-end, it is an advantage that charge-sharing between strips and common mode noise can be studied in detail, which greatly improves the understanding and performance of the detector. The equivalent noise charge (ENC) of the APV25-S1 depends on the capacitance of the strips and the de-convolution algorithm used. For our purposes, the noise is better than 2000 electrons. With 300 µm thick silicon sensors this will give a signal-to-noise ratio of better than 11:1 based on the most probable energy deposition by a minimum ionizing particle (MIP). The nominal power consumption of the APV25-S1 chip is 2.39 mW per channel, i.e. about 0.3 W per chip. The chips have been fabricated in a radiation hard deep sub-micron (0.25 μm) process.

1.3.3 Hybrids and Modules

The layout of an IST module can be seen in Figure 6. The hybrid carries 2 sensors and 12 readout chips. There will be a gap of 400 μm between the sensors. Overlapping the sensors would lead to complications in the assembly process. These acceptance gaps will be compensated because of the redundancy between SSD and IST. An interesting feature, which is not visible in this picture, is that the cable will be folded over to the backside of the ladder on which this module will be mounted. In this way the cables do not obscure visual access to the modules, which is needed for spatial survey purposes and inspection.



[1] M.J. French et al., Nucl. Instrum. Meth. A466, 359 (2001).

Figure 6: Layout of an IST module.

To keep the material budget low the IST hybrids and modules have to be constructed from low mass materials. Figure 7 shows a promising prototype Kapton hybrid design with an integrated long Kapton cable. Both hybrid and cable are about 70 µm thick. The hybrid will have to be laminated onto a proper substrate material to achieve enough mechanical rigidity. Carbon-carbon and carbon fiber are being prototyped to study their mechanical and thermal properties. In the final design the flexible cable will be long enough to be connected to more standard cables outside the active area.

For this prototype four PHOBOS Inner Vertex sensors were used because there were no IST prototype sensors produced yet and because the PHOBOS sensors are very close to the sensors used in the IST. The PHOBOS sensors are silicon pad sensors with 512 active elements per sensor, the elements are AC coupled to the 2nd metal signal traces that connect to the bonding pads. The Kapton hybrid was laminated to a 500 μm thick carbon-carbon substrate. Power, control and readout connections were wire bonded to the hybrid. As a first test only $\frac{1}{4}$ of the sensor elements were wire bonded to the readout chips. First tests show that the chips are functional and that the sensors are being read out as expected.

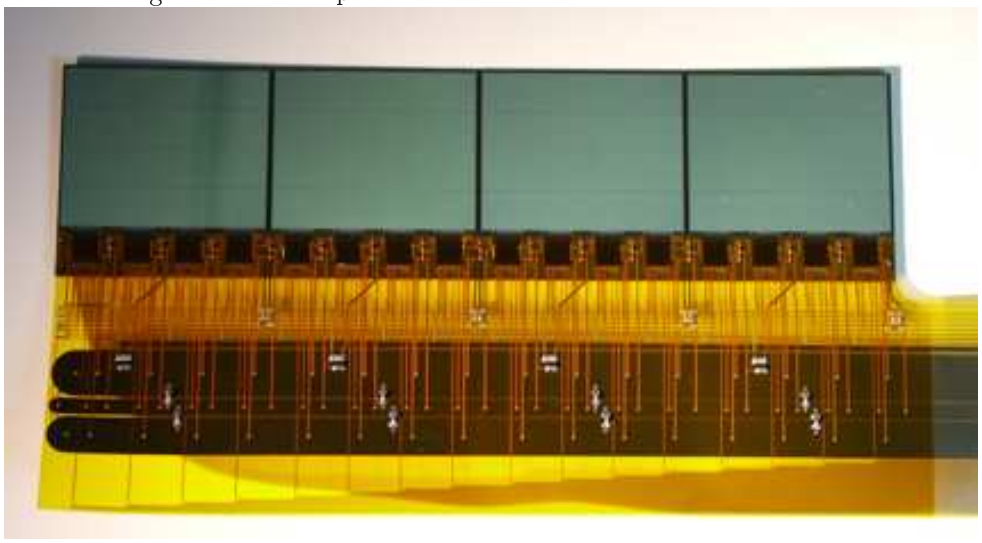


Figure 7: IST prototype with 4 PHOBOS IV sensors and 16 APV25-S1 readout chips.

1.3.4 Mechanical Support Structure

The IST barrel will consist of 24 ladders, which are mounted on a carbon fiber support cylinder. This Middle Support Cylinder (MSC) is described in Section Error: Reference source not found.

Figure 8: Long IST prototype ladder made out of carbon fiber honeycomb and carbon fiber skins. This prototype has one cooling channel.

This ladder is a shorter version of the staves under development for the ATLAS tracking upgrade. Because they are shorter they are even more rigid than the ATLAS staves and it is expected that their midpoint sag will be less than 100 μm when only end supports are used. A prototype ladder has been produced, as shown in Figure 8, and is being tested.

A more detailed cross-section of the ladder and mounted modules can be found in Figure 9. This design shows the 300 μm thick silicon sensor, the 300 μm thick APV25-S1 readout chip, the 100 μm thick Kapton hybrid-cable, the 500 μm thick carbon-carbon substrate and the 5 mm thick carbon fiber ladder with cooling tube. It also shows nicely how the Kapton hybrid folds over to the backside of the ladder where it is routed out to the readout system. The carbon-carbon substrate not only gives mechanical rigidity to the module, but also acts as a heat sink to transport heat from the readout chips to the cooling tube in the ladder.

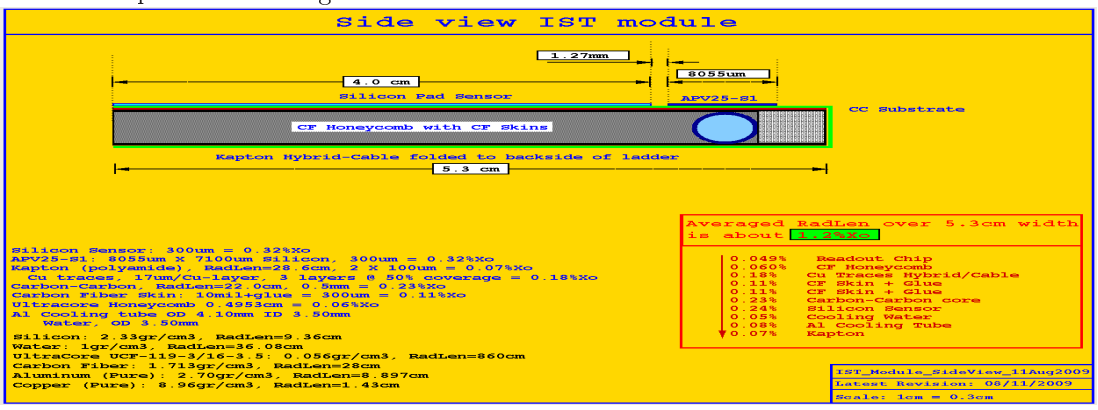


Figure 9: Cross-section of the ladder and modules. The Kapton hybrid shown in green is folded over to the back side.

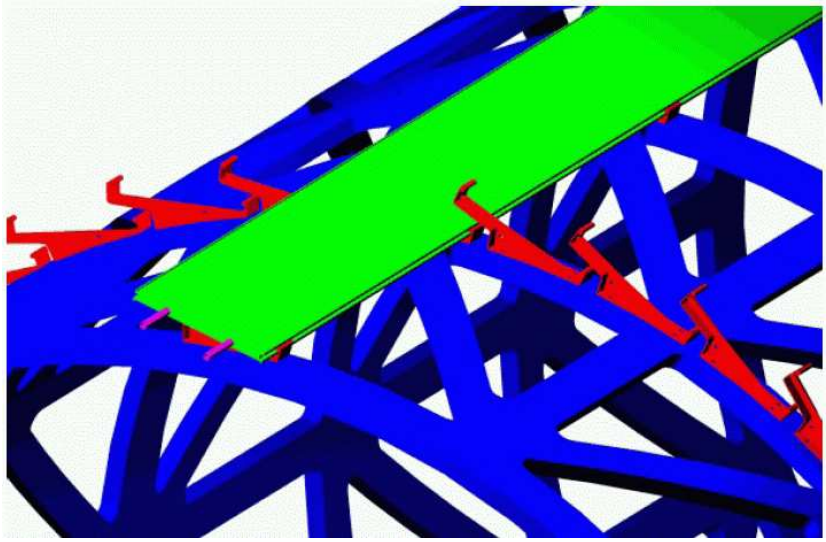


Figure 10: Ladder 'clip' mounting of the IST ladders onto the supporting cylinder (ISC).

It is expected that the ladder mounting scheme will follow the ATLAS upgrade design efforts. Figure 10 shows a schematic impression of the ATLAS mounting scheme. Here the ladders are mounted with clips on the MSC. Because of the shorter length of the IST ladders it is sufficient to use endpoint supports only. One end of the ladder would be kept fixed while the other end allows thermal expansion. A clamshell interface is required on which the ladders are mounted first. This clamshell can then be optically surveyed to determine the sensor positions before it is being mounted on the ISC.

A prototype of this clip-on design has been prepared, as shown in Figure 11, and is currently under investigation.

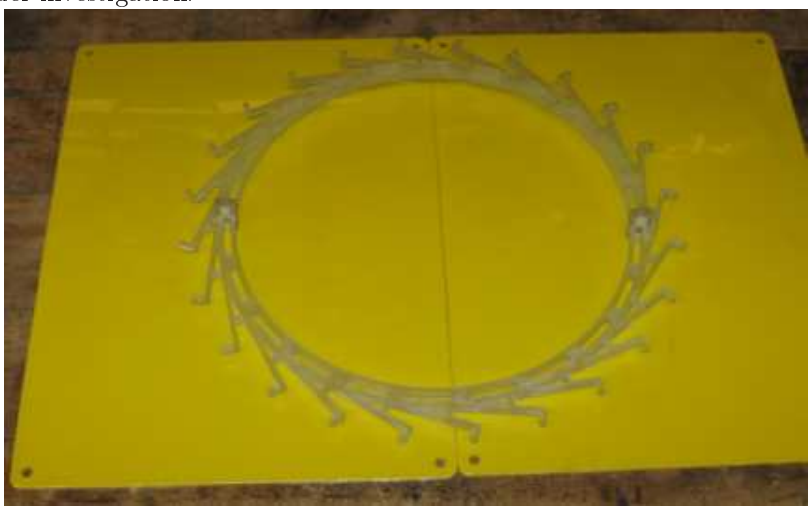


Figure 11: Rapid prototype of the IST ladder mounting structure.

The mechanical support structure will be manufactured with an overall accuracy of 100 μm. Locally, the structure supporting the IST requires an accuracy of less than 100 μm. For instance, the mounting surfaces of the sensor modules will have to be flat to within 50 μm to avoid stress on the sensors.

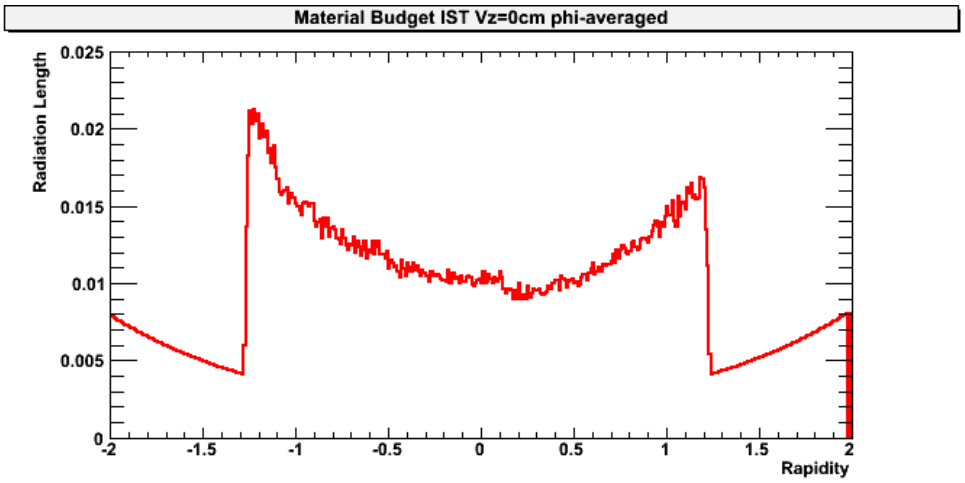


Figure 12: Phi averaged material budget for the IST as a function of rapidity.

Figure 12 provides a realistic estimate of the IST material budget by describing ladder and module designs in a GEANT geometry. These results were obtained by propagating 100,000 geantino events through the IST geometry using GEANT 3.21/08. The material budget at mid-rapidity is well below the required 1.5% X_0. The MSC and support clips where not included in this calculation. The Kapton readout cables only running in the negative rapidity direction causes the asymmetry in the material budget.

1.3.5 Cooling

The only source of dissipation on the ladders is the 36 APV25-S1 readout chips. Although the nominal power consumption is about 300 mW per chip, the final power consumption depends on the capacitance of the attached sensor channels and consequently the optimal settings of the chip parameters. For safety margin a maximum dissipation of 400 mW per chip is assumed. This leads to a dissipation of about 15 watt per ladder, 360 watt for the whole IST barrel. Trying to cool this with air only was considered too daunting and liquid cooling channels were incorporated in the ladder design. The power dissipation of 15 Watts per ladder leads to about 0.6 mW per mm^2 dissipation if the heat would spread out isotropically. The placement of the cooling tube directly under the readout chips and the use of high thermal conductive material like carbon foam will make the cooling of the ladders manageable with a room temperature cooling system. Calculations making use of FloWorks and SolidWorks are underway to determine the optimal cooling configuration. Figure 13 shows a simulation for a Freon cooled IST ladder incorporating a flattened cooling tube. In this picture the color coded temperature is displayed, showing that the APV25-S1 readout chips heat up to about 89° F (32° C). Most of the ladder remains at about 25°C.

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Figure 13: FloWorks simulation of a liquid cooled IST ladder.

1.4 Readout System, DAQ Interfacing and Slow Controls

Two customized Wiener VME readout crates will house the 36 readout boards (ARM) and 6 crate controller boards (ARC). The boards are of standard 6U x 220 mm size; the crate interconnects these boards with standard 7-slot passive CPCI backplanes and provides integrated low noise 5 V power supplies. The crate will be mounted on the south electronics platform next to the STAR detector. Each ARM handles two detector cables (24 APV chips), providing an ADC, data buffering and control of APV chip triggering and readout sequencing. The APV chip sample clock is 37.532 MHz, phase-locked to the RHIC bunch crossing (9.383 MHz). This stable timing ensures stable

effective gain without the necessity of a timing correction. The ARM also provides the I^2C slow controls interface and isolated low-voltage power supplies to the detector. The ARC interfaces to the STAR trigger and to STAR DAQ via the ALICE Detector Data Link (DDL) Source Interface Units (SIU), the standard for all new STAR DAQ-connected developments for the DAQ1000, Time of Flight (TOF), Barrel (BTOW), Forward GEM Tracker (FGT) and Endcap (ETOW) tower level 2 upgrade. The readout system can buffer up to 4096 events (the maximum number of outstanding events in STAR) and therefore decouples the IST dead time from the data acquisition system, providing a simple fixed dead time. The dead time depends on operating configuration but will typically be 11 µs, with a maximum of 26 µs. A Linux box will be located in the STAR DAQ room and fitted with the ALICE DDL receiver boards and a Myrinet interface to the event builder computer. A schematic detailing these connections is shown in Figure 14.

The slow controls system will serve as the primary means for controlling and monitoring the working parameters of the IST. These parameters, such as the hybrid temperature, component currents and voltages will be interfaced with the standard STAR alarm system. The alarm system logs the parameter history and alerts the shift crew if operating limits are exceeded. The black dashed lines in Figure 15 show the communication flow between the slow controls computer and the hardware being controlled. The red solid lines represent the actual hardware connections, which allow this communication. The slow controls for the IST detector and readout crates will be handled exclusively by Ethernet traffic to the IST Linux box, through the ALICE DDL link to the readout crates, and then finally through the RDOs to the APV's via the local I^2C link. There will be no other hardware needed for slow controls. All power supplies will be fitted with an Ethernet controls interface.

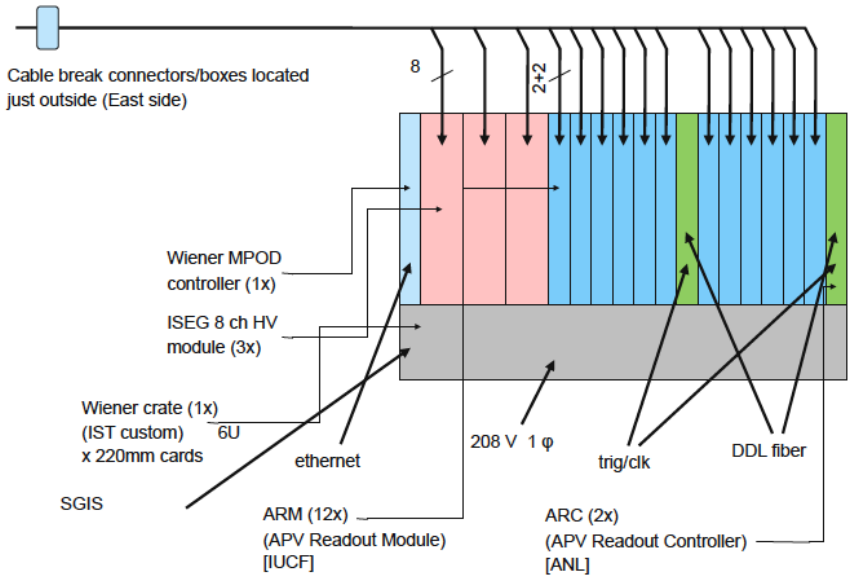

Figure 14: IST DAQ block diagram.

Although STAR is using EPICS as its standard slow control system there is a slight preference to use LabVIEW instead. LabVIEW provides the user with virtually any instrument driver and a very convenient user interface. LabVIEW runs on both Windows and Linux. It is relatively simple to interface LabVIEW and EPICS. At the moment, both options are still open.

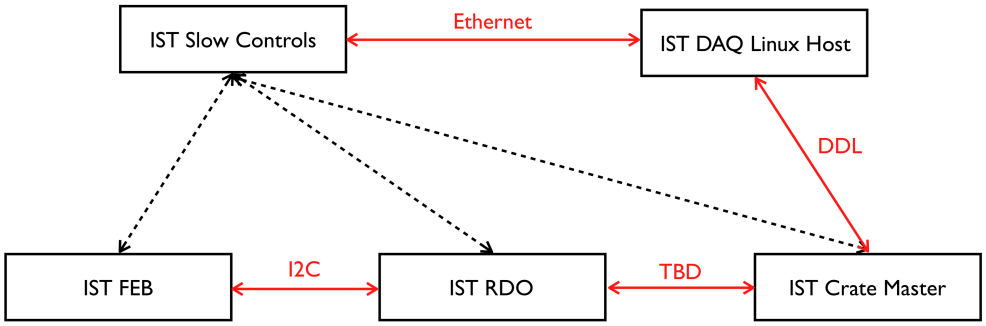

Figure 15: IST slow controls flow diagram.

1.5 Spatial Survey and Alignment

The IST will have to be aligned with respect to other detector subsystems of the inner tracking upgrade, PXL and SSD. The final alignment will be done with tracks through an iterative residual method. However, for this method to be successful it is important that the positions of the active elements are known in advance with an accuracy comparable to the resolution of the detectors. A 5-step plan can achieve this.

The positions of the sensors on the module have to be determined. Internally the structure of the sensors will be known with an accuracy of about 1 to 2 μm. This information is obtained through the production mask drawings of the sensors and accessed through alignment marks on the sensors. The modules will be built on an assembly machine under control of an operator checking the process under a microscope. The expected placing accuracy is 5 μm. After the modules have been assembled they can be surveyed with an optical survey machine at MIT. The accuracy of this machine is about 10 μm in-plane. An out-of-plane contrast measurement leads to an accuracy of 50 to 100 μm.

The same methods will be used for the ladders. Three modules will be glued to one ladder with an accuracy of about 5 μm. Then the ladder will be optically surveyed with an in-plane accuracy of 10 µm and an out-of-plane accuracy of 50 to 100 μm. After the ladder is approved it will be shipped to BNL where an additional survey will take place.

At BNL the ladders will be put together in 2 clamshell cylinders that can be measured on a coordinate measuring machine. After the clamshells have been put together on the ISC to form the IST barrel another survey needs to take place. Up to this point it should be possible to survey the silicon sensors themselves. The sensors have the highest internal accuracy (1 to 2 μm) and in the end it is their position, which should be known with the best accuracy. However, after the clamshell has been closed visual access to the sensors will become impossible, especially after the ISC gets integrated with the rest of the inner tracking system. It is important to have survey points on the ladders, the clamshell structure and the ISC, which are visible to the BNL survey group. These survey points then 'anchor' the IST inside the inner tracking system and finally to the whole STAR detector.